High-Speed Digitizer Signal Processing Option: Block Statistics (Peak Detect)

- Peak detection and Statistics functions are performed in the on-board FPGA
- Achieve data reduction and shorter transfer times to the host PC
- No waveform length limit (up to the size of the on-board memory)
- Throughput of more than 5,000,000 waveforms per second
- Peak detection is performed simultaneous on all channels
- Fully compatible with Star-Hub synchronization
- DM4i.44xx/M4x.44xx/DN2.44x/DN6.44x dead time between waveforms:
  40 samples = 80 ns at 500 MS/s or 400 ns at 100 MS/s
- M4i.22xx/M4x.22xx/DN2.22x/DN6.22x dead time between waveforms: 80/160/320 samples = 64 ns at 5 GS/s,
  64 ns at 2.5 GS/s or 64 ns at 1.25 GS/s
- Fully compatible with Spectrum API which allows programming with C/C++, Delphi, Basic, LabVIEW, MATLAB and many more.
- Available for all high-speed digitizers based on M4i and M4x technology (including digitizerNETBOX products)

Application Examples

- Ultrasonic Test
- Laser Ranging
- Medical Imaging
- Optical Fiber Test
- Mass Spectroscopy
- Component Testing
- Nanotechnology

Digitizer Models with Firmware Options

Product	Interface	Resolution	Channels	Speed	Block Average	Block Statistics	Boxcar Average
M4i.2234/2233/2230-x8	PCI Express x8	8 Bit	1/2/4 channels	5 GS/s	available	available	not available
M4i.2223/2221/2220-x8	PCI Express x8	8 Bit	1/2 channels	2.5 GS/s	available	available	not available
M4i.2212/2211/2210-x8	PCI Express x8	8 Bit	1/2/4 channels	1.25 GS/s	available	available	not available
M4x.2234/2233/2230-x4	PXI Express x4	8 Bit	1/2/4 channels	5 GS/s	available	available	not available
M4x.2223/2221/2220-x4	PXI Express x4	8 Bit	1/2 channels	2.5 GS/s	available	available	not available
M4x.2212/2211/2210-x4	PXI Express x4	8 Bit	1/2/4 channels	1.25 GS/s	available	available	not available
DN2.225-04/08	Ethernet/LXI	8 Bit	2/4/8 channels	5 GS/s	available	available	not available
DN2.223-02	Ethernet/LXI	8 Bit	2 channels	5 GS/s	available	available	not available
DN2.222-02/04	Ethernet/LXI	8 Bit	2/4 channels	2.5 GS/s	available	available	not available
DN2.221-02/04/08	Ethernet/LXI	8 Bit	2/4/8 channels	1.25 GS/s	available	available	not available
DN6.221-12/16/20/24	Ethernet/LXI	8 Bit	12/16/20/24 channels	1.25 GS/s	available	available	not available
DN6.225-12/16/20/24	Ethernet/LXI	8 Bit	12/16/20/24 channels	5 GS/s	available	available	not available
M4i.4450/4451-x8	PCI Express x8	14 Bit	2/4 channels	500 MS/s	available	available	available
M4i.4420/4421-x8	PCI Express x8	16 Bit	2/4 channels	250 MS/s	available	available	available
M4i.4410/4411-x8	PCI Express x8	16 Bit	2/4 channels	130 MS/s	available	available	available
M4x.4450/4451-x4	PXI Express x4	14 Bit	2/4 channels	500 MS/s	available	available	available
M4x.4420/4421-x4	PXI Express x4	16 Bit	2/4 channels	250 MS/s	available	available	available
M4x.4410/4411-x4	PXI Express x4	16 Bit	2/4 channels	130 MS/s	available	available	available
DN2.445-02/04/08	Ethernet/LXI	14 Bit	2/4/8 channels	500 MS/s	available	available	available
DN2.442-02/04/08	Ethernet/LXI	16 Bit	2/4/8 channels	250 MS/s	available	available	available
DN2.441-02/04/08	Ethernet/LXI	16 Bit	2/4/8 channels	130 MS/s	available	available	available
DN6.445-12/16/20/24	Ethernet/LXI	14 Bit	12/16/20/24 channels	500 MS/s	available	available	available
DN6.442-12/16/20/24	Ethernet/LXI	16 Bit	12/16/20/24 channels	250 MS/s	available	available	available
DN6.441-12/16/20/24	Ethernet/LXI	16 Bit	12/16/20/24 channels	130 MS/s	available	available	available

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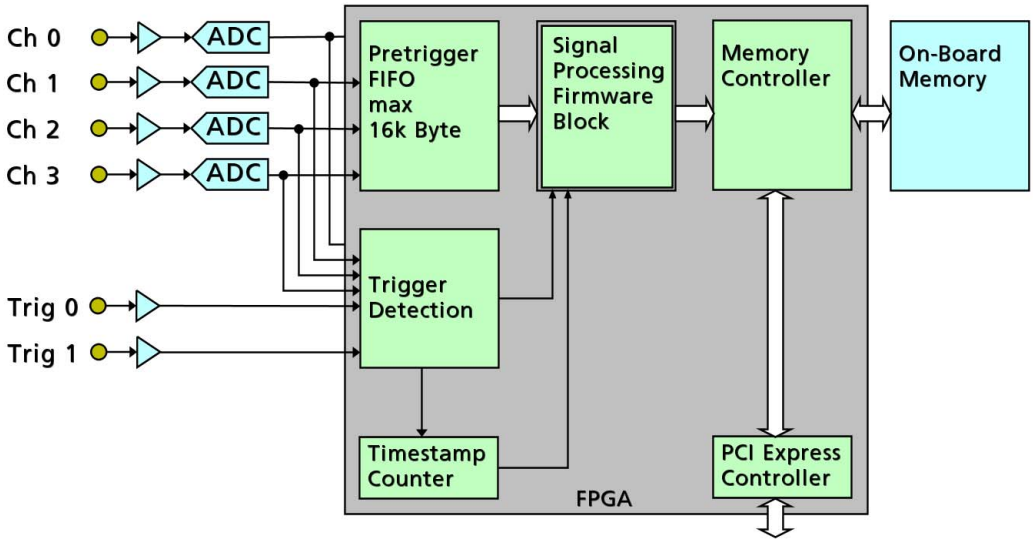
Simplified Block Diagram

The following block diagram shows the general structure and data flows of the M4i/M4x based digitizer hardware. When running in the standard digitizer configuration the signal processing block simply consists of a bypass handing the input data to the memory controller without further calculations.

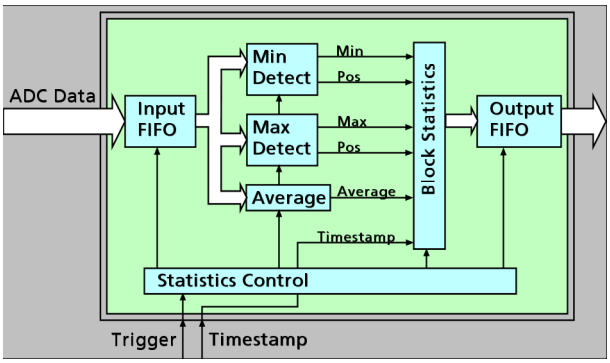


General Information

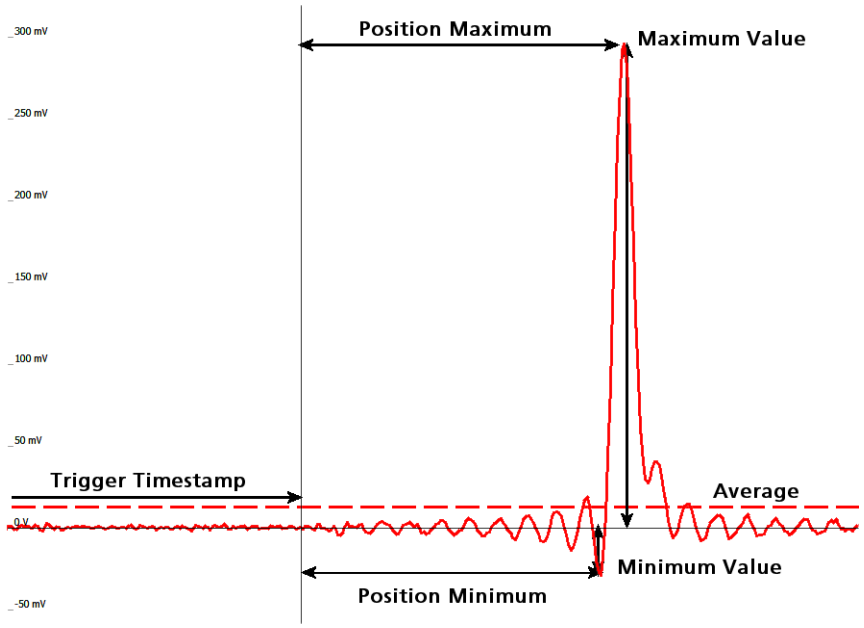
The Block Statistics and Peak Detection Module implements a widely used data analysis and reduction technology in hardware. Each block is scanned for its minimum and maximum peak and a summary date set that includes the minimum, maximum, average, timestamps and position information is stored in memory.

The complete Block Statistics and Peak Detection process is done inside the FPGA of the digitizer producing no CPU load at all. This data reduction process decreases the amount of data that needs to be transferred to the host PC further reducing CPU demand and speeding up measurement times.

The signal processing firmware also includes the standard digitizer firmware so that normal digitizer operation can be performed with no limitations.



Waveform Block Statistics



Information Set	
Average Value	64 Bit signed integer
Minimum Value	16 Bit signed integer
Maximum Value	16 Bit signed integer
Minimum Position	32 Bit unsigned integer
Maximum Position	32 Bit unsigned integer
Unused	32 Bit
TriggerTimestamp	64 Bit unsigned integer

Technical Data

Block Statistics Signal Processing Option M4i.22xx/DN2.22x Series/DN6.22x Series

Minimum Waveform Length		64 samples
Minimum Waveform Stepsize		32 samples
Maximum Waveform Length	Standard Acquisition	2 GSamples / channels
Maximum Waveform Length	FIFO Acquisition	2 GSamples
Data Output Format	fixed	32 bytes statistics summary
Statistics Information Set per Waveform		Average, Minimum, Maximum, Position Minimum, Position Maximum, Trigger Timestamp
Re-Arming Time between Segments	1.25 GS/s or below	80 samples (+ programmed pretrigger)
Re-Arming Time between Segments	2.5 GS/s	160 samples (+ programmed pretrigger)
Re-Arming Time between Segments	5 GS/s	320 samples (+ programmed pretrigger)

Block Statistics Signal Processing Option M4i.44xx/M4x.44xx/DN2.44x/DN6.44x Series

Minimum Waveform Length		32 samples
Minimum Waveform Stepsize		16 samples
Maximum Waveform Length	Standard Acquisition	2 GSamples / channels
Maximum Waveform Length	FIFO Acquisition	2 GSamples
Data Output Format	fixed	32 bytes statistics summary
Statistics Information Set per Waveform		Average, Minimum, Maximum, Position Minimum, Position Maximum, Trigger Timestamp
Re-Arming Time between Segments		40 samples (+ programmed pretrigger)

Order Information digitizerNETBOX Models

Firmware Options

Order no.	Option
DN2.xxx–spavg	Signal Processing Firmware Option: Block Average (later installation by firmware - upgrade available)
DN2.xxx-spstat	Signal Processing Firmware Option: Block Statistics/Peak Detect (later installation by firmware - upgrade available)
DN6.xxx-spavg	Signal Processing Firmware Option: Block Average (later installation by firmware - upgrade available)
DN6.xxx-spstat	Signal Processing Firmware Option: Block Statistics/Peak Detect (later installation by firmware - upgrade available)

Order Information M4i and M4x Card Models

Firmware Options

Order no.	Option
M4i.xxxx–spavg	Signal Processing Firmware Option: Block Average (later firmware - upgrade available)
M4i.xxxx-spstat	Signal Processing Firmware Option: Block Statistics/Peak Detect (later firmware - upgrade available)