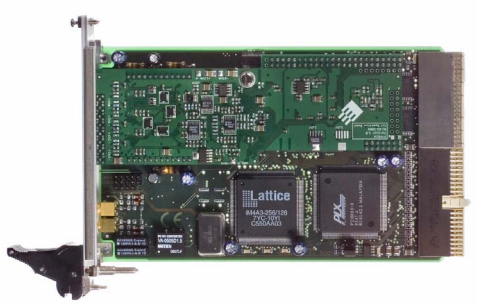
SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MX.49xx - four channel 16 bit high-speed A/D

- **PXI 3U / CompactPCI 3U format**
- **4 channels with up to 10 MS/s, 25 MS/s or 50 MS/s**
- **True differential / single-ended selectable**
- **Simultaneously sampling on all channels**
- **Separate ADC and amplifier per channel**
- **6 input ranges: ±200 mV up to ±10 V**
- **Programmable input offset of ±100% V**
- **Complete on-board calibration**
- **Up to 64 MSample (128 MByte) on-board memory**
- **Additional digital inputs as option available**
- **Window/pulsewidth trigger**
- **Synchronization possible**



Product range overview

Model	1 channel	2 channels	4 channels
MX.4911	10 MS/s SE 10 MS/s Diff	10 MS/s SE 10 MS/s Diff	10 MS/s SE
MX.4931	25 MS/s SE 25 MS/s Diff	25 MS/s SE 25 MS/s Diff	25 MS/s SE
MX.4963	50 MS/s SE 50 MS/s Diff	50 MS/s SE 50 MS/s Diff	25 MS/s SE

Software/Drivers

A large number of drivers and examples are delivered with the board:

- Windows NT/2000 32 bit drivers
- Windows XP/Vista/7/8/10, 32 and 64 bit driver
- Linux 32bit and 64bit drivers
- SBench 6.x Base version for Windows and Linux
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic & Excel examples
- Python examples
- LabWindows/CVI examples
- LabVIEW - drivers and examples
- MATLAB - drivers and examples
- Other 3rd party drivers (e.g. VEE,DASYLab) are partly available upon request

General Information

The MX.49xx cards allow recording of up to four channels with sampling rates of 25 MS/s or two channels with sampling rates of 50 MS/s. These cards offer outstanding A/D features both in resolution and speed for PXI. The cards can be switched between Single-Ended inputs with a programmable offset and true differential inputs. If used in differential mode each two inputs are connected together reducing the number of available channels by half. The 16 bit vertical resolution has four times the accuracy compared to 14 bit cards and sixteen times the accuracy compared with a 12 bit card.
All boards of the MX.49xx series may use the whole installed on-board memory of up to 64 MSamples, completely for the currently activated number of channels.

Software programmable parameters

Sampling rate	10 kS/s to max sampling rate, external clock, ref clock, PXI clock
Input range	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input Offset (single-ended)	programmable to ±100% in steps of 1%
Input type	Single-ended, true differential
Clock mode	internal PLL, internal quartz, external reference clock, PXI reference clock
Clock impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger mode	Channel, External, Software, Auto, Window, Pulse, PXI Line[5..0], PXI Startrigger
Trigger level resolution	14 bit
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is posible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

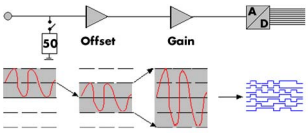
PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software commend one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

Input Amplifier

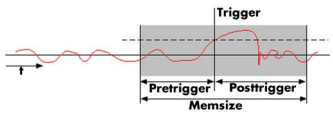


The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

Automatic on-board calibration

All of the channels are calibrated in factory before the board is shipped. To compensate for different variations like PC power supply, temperature and aging, the software driver provides routines for an automatic onboard offset and gain calibration of all input ranges. All the cards contain a high precision on-board calibration reference.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

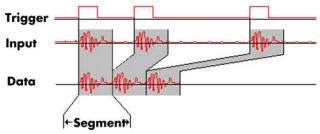
External trigger I/O

All instruments can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

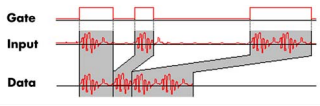
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording mode allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

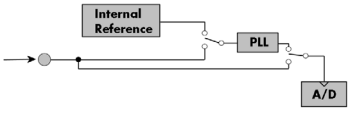


The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock output

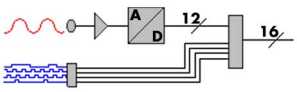
Using a dedicated connector it is possible to output the internally used sampling clock to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 16 additional digital inputs on 4 channel A/D instruments and 32 digital inputs on A/D instruments with 8 and more channels.

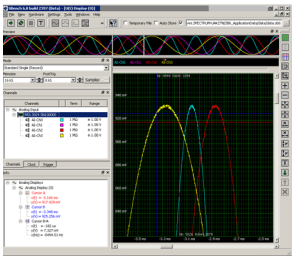
The digital inputs can be mulitplexed into the analog data by software command using many different formats:

- Each 16 digital inputs can replace one analog channel.
- Each 2 digital inputs can be multiplexed into an analog channel with a resolution reduced to 14 bit.
- Each 4 digital inputs can be multiplexed into an analog channel with a resolution reduced to 12 bit.

Differential inputs

With a simple software command the inputs can individually be switched from single-ended (in relation to ground) to differential by combining each two single-ended inputs to one differential input. When the inputs are used in differential mode the A/D converter measures the difference between two lines with relation to system ground.

SBench 6



A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, display acquired data and make some basic measurements. It's a valuable tool for checking the card's performance and assisting with the unit's initial setup. The cards also come with a demo license for the SBench 6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all acquisition modes including data streaming. Data streaming allows the cards to continuously acquire data and transfer it directly to the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE, GNOME and Unity) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

Technical Data

Analog Inputs

Resolution		16 bit (can be reduced to acquire simultaneous digital inputs)
Input Range	software programmable	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input Type	software programmable	Single-ended or True Differential
Input Offset (single-ended)	software programmable	programmable to ±100% of input range in steps of 1%
ADC Differential non linearity (DNL)	ADC only	491x + 493x: ±1.2 LSB; 496x: ±1.4 LSB
ADC Integral non linearity (INL)	ADC only	491x + 493x: ±5.5 LSB; 496x: ±6.5 LSB
Offset error (full speed)	after warm-up and calibration	≤ 0.1%
Gain error (full speed)	after warm-up and calibration	≤ 0.1%
Crosstalk: Signal ≤ 1 MHz, 50 ohm	range ≤ ±1V	≤ 100 dB on adjacent channels (all card types)
Crosstalk: Signal ≤ 1 MHz, 50 ohm	range ≥ ±2V	≤ 58 dB on adjacent channels (M2i.491x, M2i.493x, M2i.4963, M2i.4964)
Crosstalk: Signal ≤ 1 MHz, 50 ohm	range ≥ ±2V	≤ 80 dB on adjacent channels (M2i.4960, M2i.4961)
Analog Input impedance	software programmable	50 Ohm / 1 MOhm || TBD pF
Analog input coupling	fixed	DC
Over voltage protection	range ≤ ±1V	±5 V
Over voltage protection	range ≥ ±2V	±40 V
CMRR (Common Mode Rejection Ratio)	range ≤ ±1V	100 kHz: 80 dB, 1 MHz: 59 dB, 10 MHz: 41 dB
CMRR (Common Mode Rejection Ratio)	range ≥ ±2V	100 kHz: 59 dB, 1 MHz: 53 dB, 10 MHz: 52 dB
Channel selection (single-ended inputs)	software programmable	1, 2, 4, 8 or 16 channels (maximum is model dependent)
Channel selection (true differential inputs)	software programmable	1, 2, 4 or 8 channels (maximum is model dependent)

Trigger

Available trigger modes	software programmable	Channel Trigger, External, Software, Window, Pulse, Re-Arm, Spike, Or/And, Delay
Trigger level resolution	software programmable	14 bit
Trigger edge	software programmable	Rising edge, falling edge or both edges
Trigger pulse width	software programmable	0 to [64k - 1] samples in steps of 1 sample
Multi, Gate: re-arming time		< 20 samples
Pretrigger at Multi, ABA, Gate, FIFO		Fixed value depending on channel settings and sampling rate
Posttrigger	software programmable	[32 / channels] up to [128M / channels] in steps of [32 / channels]
Memory depth	software programmable	[32 / channels] up to [memory / channels] samples in steps of [32 / channels]
Multiple Recording segment size	software programmable	[32 / channels] up to [installed memory / 2 / channels] samples in steps of [32 / channels]
Trigger output delay		One positive edge after internal trigger event
Internal/External trigger accuracy		1 sample
External trigger type (input and output)		3.3V LVTTL compatible (5V tolerant)
External trigger input		Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 8 ns in pulse stretch mode, ≥ 2 clock periods all other modes
External trigger maximum voltage		-0.5 V up to +5.7 V (internally clamped to 5.0V, 100 mA max. clamping current)
Trigger impedance	software programmable	50 Ohm / high impedance (> 4kOhm)
External trigger output levels		Low ≤ 0.4 V (@ 20 mA, max 64 mA), High ≥ 2.4 V (@ -20 mA, max -48 mA), TTL compatible
External trigger output drive strength		Capable of driving 50 ohm load

Clock

Clock Modes	software programmable	internal PLL, internal quartz, external. clock, external divided, external reference clock, sync
Internal clock range (PLL mode)	software programmable	1 kS/s to max using internal reference, 50kS/s to max using external reference clock
Internal clock accuracy		≤ 50 ppm
Clock Divider Value for external divided mode	software programmable	1, 2, 4, 8, 10, 16, 20, 40, 50, 80, 100, 200, 400, 500, 800, 1000, 2000
External reference clock range	software programmable	≥ 1.0 MHz and ≤ 125.0 MHz
External clock impedance	software programmable	50 Ohm / high impedance (> 4kOhm)
External clock range		see table below
External clock delay to internal clock		5.4 ns
External clock type/edge		3.3V LVTTL compatible, rising edge used
External clock input		Low level ≤ 0.8 V, High level ≥ 2.0 V, duty cycle: 45% - 55%
External clock maximum voltage		-0.5 V up to +3.8 V (internally clamped to 3.3V, 100 mA max. clamping current)
External clock output levels		Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength		Capable of driving 50 ohm load
Synchronization clock divider	software programmable	2 up to [8k - 2] in steps of 2

PXI Features

PXI Reference Clock Input	software programmable	Supported as reference clock input
PXI Star Trigger Input	software programmable	Supported as trigger source
PXI Trigger Bus	software programmable	Supporting PXI_TRIG[0] to PCI_TRIG[5] as either trigger input or trigger output

Digital Inputs Option

Digital data acquisition modes	software programmable	per channel: ADC 16 bit, ADC 14 bit + 2 DI, ADC 12 bit + 4 DI, replace ADC with 16 DI
Digital inputs delay to analog sample		0 Samples
Input Impedance		> 4,7 kOhm with Bus-Hold circuity, unused inputs can be left floating, override current ≥ 500 µA
Maximum voltage		-0.3 V up to +5.5 V (internally clamped to 3.3V and ground, 200 mA max. clamping current)
Input voltage		Low ≤ 0.8 V, High ≥ 2.0 V (TTL compatible)

Connectors

Analog Inputs		3 mm SMB male (one for each single-ended input)	Cable-Type: Cab-3f-xx-xx
Trigger Input/Output	programmable direction	3 mm SMB male (one connector)	Cable-Type: Cab-3f-xx-xx
Clock Input/Output	programmable direction	3 mm SMB male (one connector)	Cable-Type: Cab-3f-xx-xx
Option Digital Inputs		40 pole half pitch (Hirose FX2 series)	Cable-Type: Cab-d40-xx-xx

Environmental and Physical Details

Dimension (PCB only)	160 mm x 100 mm (Standard 3U)
Width (Standard)	1 slot
Width (with option Digital Inputs)	additionally extra bracket on neighbour slot
Warm up time	10 minutes
Operating temperature	0°C to 50°C
Storage temperature	-10°C to 70°C
Humidity	10% to 90%

Certification, Compliance, Warranty

PXI bus slot type	32 bit 33 MHz
PXIe hybrid slot compatibility	Not compatible
EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	2 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge

Power Consumption

Max Power Consumption @ 3.3V	3.3 A
Max Power Consumption @ 5V	1.2 A

MTBF

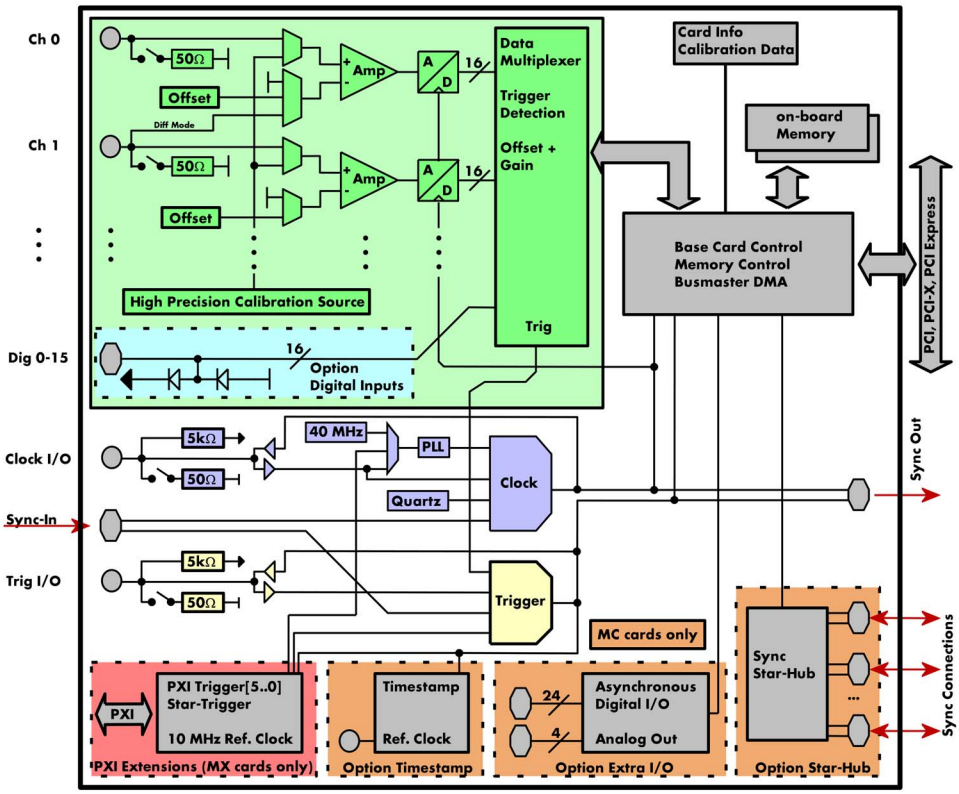
MTBF	TBD

Dynamic Parameters

	MX.4911 MC.4911 MC.4912	MX.4931 MC.4931 MC.4932	MX.4963 MC.4963 MC.4964
Min internal clock (PLL)	10 kS/s	10 kS/s	10 kS/s
Min internal clock (Quartz)	50 kS/s	50 kS/s	50 kS/s
Max sampling rate	10 MS/s	25 MS/s	50 MS/s
Min external reference clock	1 MHz	1 MHz	1 MHz
Min external reference clock	125 MS/s	125 MS/s	125 MS/s
-3 dB bandwidth	>5 MHz	>15 MHz	>30 MHz
Zero noise level (Range ±200 mV and ±2V)	< 5.0 LSB rms	< 5.5 LSB rms	< 7.0 LSB rms
Zero noise level (all other ranges)	< 4.0 LSB rms	< 4.5 LSB rms	< 5.0 LSB rms
Test - sampling rate	10 MS/s	25 MS/s	50 MS/s
Test signal frequency	1 MHz	1 MHz	1 MHz
SNR (typ)	≥ 76.3 dB	≥ 76.0 dB	≥ 75.6 dB
THD (typ)	≤ -80.5 dB	≤ -80.5 dB	≤ -80.0 dB
SFDR (typ), excl. harm.	≥ 92.4 dB	≥ 92.0 dB	≥ 92.0 dB
ENOB (based on SNR)	≥ 12.3 LSB	≥ 12.2 LSB	≥ 12.2 LSB
ENOB (based on SINAD)	≥ 12.2 LSB	≥ 12.2 LSB	≥ 12.1 LSB

Dynamic parameters are measured at ±5 V input range (if no other range is stated) and 1 MOhm termination with the sampling rate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Hardware block diagram



Order Information

The card is delivered with 32 MSample on-board memory and supports standard mode (Scope), FIFO mode (streaming), Multiple Recording and Gated Sampling. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows), LabWindows/CVI, Delphi, Visual Basic, Python and a Base license of the oscilloscope software SBench 6 are included. Drivers for other 3rd party products like VEE or DASYLab may be available on request.

Adapter cables are not included. Please order separately!

Versions

Order no.	Standard mem	1 channel	2 channels	4 channels
MX.4911	32 MSample	10 MS/s	10 MS/s	10 MS/s
MX.4931	32 MSample	25 MS/s	25 MS/s	25 MS/s
MX.4963	32 MSample	50 MS/s	50 MS/s	25 MS/s

Memory

Order no.	Option
MX.4xxx-64M	Memory upgrade to 64 MSample (128 MB) of total memory
MX.4xxx-up	Additional fee for later memory upgrade

Options

Order no.	Option
M2i.49xx-dig	Additional synchronous digital inputs with multiple data formats (16 digital channels on 2 and 4 channel cards and 32 digital channels on 8 channel cards) including Cab-d40-idc-100

Cables

		Order no.					
for Connections	Length	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female	
Analog/Clock/Trigger	80 cm	Cab-3f-9m-80	Cab-3f-9f-80	Cab-3f-3mA-80	Cab-3f-3fA-80	Cab-3f-3f-80	
Analog/Clock/Trigger	200 cm	Cab-3f-9m-200	Cab-3f-9f-200	Cab-3f-3mA-200	Cab-3f-3fA-200	Cab-3f-3f-200	
Probes (short)	5 cm		Cab-3f-9f-5				
		to 2x20 pole IDC	to 40 pole FX2				
Digital signals (option)	100 cm	Cab-d40-idc-100	Cab-d40-d40-100				

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

Technical changes and printing errors possible